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(54) Name of Invention: Semiconductor Substrate and Manufacturing Method Thereof

(57) [Abstract]
[Subject]
To provide a semiconductor substrate that combines a stable internal IG region and high crystallinity active device region without requiring the costly EG or IG processes.

[Method of Solution]
After performing a high-temperature epitaxial layering process at at least 1150°C, rapidly cooling of the substrate at at least 10 K/s can create enough crystal defects in the first 700 to 1000°C process in the device fabrication process to make it possible to maintain the gettering process throughout the entire device fabrication process even if no EG processes and no special IG processes for generating crystal defects are performed.

[Range of Patent Claims]

[Claim 1] A semiconductor substrate having a defect density that has an intrinsic gettering capability of 10^6 to 10^7 cm^{-2}, where said defect density is provided in the process wherein the epitaxial growth on the silicon semiconductor substrate is performed, and propagated during a subsequent thermal process.

[Claim 2] A method for manufacturing a semiconductor substrate provided with an intrinsic gettering capability within the substrate provide by the rapid cooling of said substrate at a rate of at least 10 K/s after the growth of an epitaxial layer on said silicon semiconductor substrate at at least 1150°C.

[Claim 3] The semiconductor substrate manufacturing method of Claim 2, where a thermal process after epitaxial growth is in a temperature range between 700 and 1000°C.

[Detailed Explanation of the Invention]

[0001]
[Technological Field of the Invention]

This invention pertains to semiconductor substrates, and to the manufacturing method thereof, where said semiconductor substrates are provided with an intrinsic gettering capability within the substrate by the introduction of internal defect nucleation sites by specific thermal processes performed during the process used to grow an epitaxial layer on the epitaxial wafers, where an epitaxial layer is grown on a substrate and this layer is used as a semiconductor substrate.

[0002]
[Prior Art]

The level of integration of today's silicon semiconductor devices is advancing rapidly, leading to increasingly challenging requirements for the silicon wafers. Crystal defects or metallic impurities (aside from the dopants) in the active device regions (i.e., the areas where the devices are fabricated) in a highly integrated device may compromise electrical performance (such as increased leakage current).

[0003]

Conventionally, highly integrated silicon semiconductor devices have used CZ-Si wafers grown using the CZ method. It is well known that these CZ-Si wafers contain on the order of 10^{18} atoms/cm^3 of supersaturated interstitial oxygen, which can cause crystal defects such as oxygen precipitation, dislocation, or stacking faults.

[0004]

Conventionally, thermal processes at high temperatures (1100 to 1200°C) for several hours duration have been used for the LOCOS fabrication or the well diffusion layer fabrication, and thus a denuded zone (DZ) layer (a layer several dozen microns thick near the surface where there are no crystal defects) is formed naturally because the interstitial oxygen near the surface of the substrate is diffused out (out gassed), naturally suppressing the occurrence of crystal defects in the active device regions on the wafer surface.

[0005]

However, as semiconductor devices have been miniaturized further, high-energy ion implantation has been used for the well formation, and the device fabrication processes are performed at lower temperatures (less than 1000°C), which are inadequate for the out-gassing of oxygen described above, making it difficult to create the DZ layer at the surface of the wafer. While low-oxygen wafers are being used in response to this issue, it is still difficult to control adequately the occurrence of crystal defects.

[0006]
[The Issues These Inventions Attempt to Solve]

Because of the above, the highly integrated devices of today often use epitaxial wafers (wafers whereon an epitaxial layer, virtually free of crystal defects, is grown). However, even given these epitaxial wafers with their nearly perfect crystals, the characteristics of the devices can still be compromised by metallic contamination in the epitaxial layer in the downstream device fabrication processes.

[0007]

It is for this reason that gettering technology, a technology which captures the metallic impurities in a location far from the active device region (called a "sink") is necessary.

Conventionally, either intrinsic gettering (IG), where the crystal defects, stemming from intrinsic oxygen, serve as the sinks during thermal processes in the device manufacturing process, or extrinsic gettering (EG), where typically the either back surface of the wafer is damaged through sandblasting or the back surface is subjected to stress through the growth of an Si_3N_4 layer or the growth of a poly-Si layer, is used.

[0008]

Because high temperature thermal processes between 1050 and 1200 °C are performed during the epitaxial process, there will be few oxygen precipitation nucleation sites remaining within the CZ-Si substrate, and these sites will be eliminated, making it difficult to evoke adequate crystal defects in the substrate in the subsequent device fabrication processes. This leads to the new problem of a reduced IG effect regarding the metallic contamination in, of course, the first phase of the device fabrication process, and then throughout the entire process.

[0009]

It is because of this that IG processes are used in addition to EG processes. In these IG processes crystal defects are created intentionally in the wafer in thermal processes about the time of the epitaxial process so that these crystal defects can be used as sinks. Because these thermal processes necessarily include high temperature processes (between 1000 and 1200°C) to control the creation of oxygen precipitants in the active device area through reducing the oxygen concentration near the surface of the wafer by out-gassing oxygen through diffusion, low temperature processes (600 to 800°C) to generate defect nuclei and mid-temperature processes (800 to 1000°C), these thermal processes are quite costly.

[0010]

Furthermore, EG processes not only increase costs, but also have the further problem of generating particulate contamination when the stress layer peels from the silicon.

[0011]

The purpose of this invention is to respond to the problems described above by providing a semiconductor substrate (and the manufacturing method thereof) that does not require the costly EG and IG processes, but rather is able to provide a combination of a stable internal IG region with a high crystallinity active device region.

[0012]

[Method for Solving the Problem]

As a result of a variety of investigations by the authors into the creation of internal IG regions and with the goal of providing a semiconductor substrate that has both a stable internal IG region and a high crystallinity active device region, the authors learned that cooling the semiconductor substrate at a rate of at least 10 K/s after growing an epitaxial layer at at least 1150 °C on the silicon wafer creates crystal defect nucleation in the internal IG region within the wafer, and thus they arrived at this invention.

[0013]

This invention provides a semiconductor substrate having a defect density that has an intrinsic gettering capability of 10^6 to 10^7 cm^{-2}, where said defect density is provided in the process wherein the epitaxial growth on the silicon semiconductor substrate is performed, and propagated during a subsequent thermal process and provides a method for manufacturing a semiconductor substrate with such an intrinsic gettering capability within the substrate, provided by the rapid cooling of said substrate at a rate of at least 10 K/s after the growth of an epitaxial layer on said silicon semiconductor substrate at at least 1150°C with, a thermal process after, for example, epitaxial growth in a temperature range between 700 and 1000°C.

[0014]

[Embodiment of the Invention]

The manufacturing method in this invention is characterized by the maintenance of the silicon wafer at a high temperature in excess of 1150°C for a specific amount time in the epitaxial growth process, after which the wafer is cooled at a specific rate to provide IG capability when the oxygen defects are propagated in the subsequent thermal process. This phenomenon occurs only when oxygen within the substrate is in a supersaturated state, and because there is no oxygen in the epitaxial layer used for the active device region, the quality of the epitaxial layer (with its extremely high crystallinity) is not degraded. Thus it is possible to obtain both a stable IG region and an active device region with excellent crystallinity.

[0015]

In this invention, the desirable temperature for epitaxial growth is between 1150°C and 1250°C, after which the cooling speed should be in a range of 10 K/s to 100 K/s. While the lower limits for the temperature range and the cooling speed are the requirements to produce crystal defects with high densities of 10^6 to 10^7 cm^{-2} in the thermal processes following the epitaxial growth process, exceeding the upper limit values will cause slippage and warp in the silicon wafer, and thus the range described above is desirable.

[0016]

The silicon wafer produced in this invention is characterized by the production high density crystal defects in the order of 10^6 to 10^7 cm^{-2} regardless of the thermal processing temperatures in the thermal processes after epitaxial growth as long as the temperature of the thermal processes is between 700 and 1000°C. This makes it possible to produce enough crystal defects during the 700 to 1000°C oxide or nitride processes that are performed at the beginning of the device fabrication process to maintain the IG effect throughout the entire device fabrication process. Consequently, the need for EG processes or for special IG processes to provide crystal damage before or after the epitaxial deposition process is eliminated, and thus this invention is extremely useful when it comes to silicon wafer manufacturing cost.

[0017]

[Example of Embodiment]

As experimental materials we prepared 8-inch CZ-Si wafers (oxygen density: 11×10^{17} atoms/cm^3) of a P-type species (100) with five different resistivities (4 m Ω cm, 7 m Ω cm, 11 m Ω cm, 50 m Ω cm, and 500 m Ω cm) using a boron dopant.

[0018]

We preformed a 60-second 1150°C bake process in a hydrogen atmosphere followed by the deposition process, using a lamp-heated horizontal CVD epitaxial reactor. The deposition process used trichlorosilane as the raw material. The depositions were performed using 180-second deposition processes at each of three different temperatures, 1100°C, 1150°C, and 1200°C, to deposit epitaxial layers approximately 3μ thick.

[0019]

After the deposition, we cooled the wafers from each of the initial temperatures at 3 different cooling speeds, 5 K/s, 10 K/s and 15 K/s. This was followed by a 16-minute thermal process at 1000°C in a dry oxygen environment, using a 2-stage thermal process where the temperature was ramped to 700°C, 800°C, or 900°C and held for four minutes, before processing at 1000°C for sixteen minutes.

[0020]

Using these test samples, we then performed a Wright etch and examined the results under an optical microscope. The observed results are shown in Figures 1 through 3, where the deposition processes were performed at 1100°C, 1150°C and 1200°C respectively. In each figure, Figure A shows the case where the cooling speed after deposition was 5 K/s, Figure B shows the case where the cooling speed was 10 K/s, and Figure C shows the case where the cooling speed was 15 K/s. The vertical axes show the defect densities while the horizontal axes indicate the first-stage temperature in the two-stage heating process in the epitaxial deposition process. The results for the 1000°C single-stage heating process are shown by the black marks in the figures.

[0021]

As is clear in Figures 1 through 3, when the epitaxial deposition process was 1100°C, and when the cooling speed was 5 K/s after an epitaxial process at 1150°C or 1200°C, the defect density falls with the higher the first-stage thermal process temperature after the epitaxial process. This is because the microscopic defects smaller than the defect viability threshold size at the respective temperatures during the epitaxial deposition process and the first-stage thermal process after the epitaxial process shrank and were eliminated, so only those nuclei greater than the threshold size propagated in the next 1000°C thermal process. The defect densities were low in these samples, and thus we can expect no intrinsic gettering effect.

[0022]

In contrast, as is shown in Figures 2 and 3, in the samples where the epitaxial deposition process temperature was 1150°C or 1200°C with a cooling speed of 10 K/s or 15 K/s, and regardless of the resistivity of the initial wafer and of the first-stage heating process temperature after the epitaxial process, we observed defect density values in the order of 10^5 to 10^7 cm^{-2} even in the 1000°C first-stage heating process (which included no low temperature nucleation process). We infer that this is because even though more defect nuclei are eliminated in the 1150°C and 1200°C epitaxial deposition process than in the 1100°C process, dropping the temperature at at least 10 K/s generated many crystal defects in the thermal processing after the epitaxial process.

[0023]

[Effects of the Invention]

As is apparent from the example of embodiment, the IG gettering effect can be increased by creating high density internal defects through controlling the cooling speed to at least 10 K/s after performing the epitaxial deposition process at at least 1150°C. In other words, it is possible to maintain a gettering effect though the entire device fabrication process even when no intrinsic gettering process is performed by which to especially generate crystal defects, and even when no extrinsic gettering process is performed. This is because it is possible to produce adequate crystal defects by performing a rapid cool process from the high temperature in the epitaxial process and following this process with a 700 to 1000°C thermal process at the start of the device fabrication process, considering the fact that the defect density is not greatly dependent on the precipitation temperature after rapid cooling from the high temperature, and considering the fact that it is possible to maintain adequately the active device region through out-gassing (outward diffusion) of oxygen during the high temperature processes in the epitaxial deposition process.

[Simple Explanation of Figures]

[Figure 1] Figure 1 is a graph showing the influence on defect density of the deposition process temperature in the epitaxial deposition process and on the cooling speed, where the vertical axis indicates the defect density and the horizontal axis indicates the first-stage thermal process temperature in the 2-stage thermal process after the epitaxial deposition process is performed. A indicates the case where the cooling speed after the epitaxial

deposition process was 5 K/s, B indicates the case where the cooling speed was 10 K/s, and C indicates the case where the cooling speed was 15 K/s, where the deposition process temperature in all cases was 1100°C.

[Figur 2] Figure 1 is a graph showing the influence on defect density of the deposition process temperature in the epitaxial deposition process and on the cooling speed, where the vertical axis indicates the defect density and the horizontal axis indicates the first-stage thermal process temperature in the 2-stage thermal process after the epitaxial deposition process is performed. A indicates the case where the cooling speed after the epitaxial deposition process was 5 K/s, B indicates the case where the cooling speed was 10 K/s, and C indicates the case where the cooling speed was 15 K/s, where the deposition process temperature in all cases was 1150°C.

[Figure 3] Figure 1 is a graph showing the influence on defect density of the deposition process temperature in the epitaxial deposition process and on the cooling speed, where the vertical axis indicates the defect density and the horizontal axis indicates the first-stage thermal process temperature in the 2-stage thermal process after the epitaxial deposition process is performed. A indicates the case where the cooling speed after the epitaxial deposition process was 5 K/s, B indicates the case where the cooling speed was 10 K/s, and C indicates the case where the cooling speed was 15 K/s, where the deposition process temperature in all cases was 1200°C.

[INSERT FIGURES 1 - 3]
[CAPTIONS FOR ALL VERTICAL AXES ON PAGES 5 THROUGH 7] Defect Density (cm^2)
[CAPTIONS FOR ALL HORIZONTAL AXES ON PAGES 5 THOUGH 7] First-stage Thermal Process Temperature (°C)

[Key] Resistivity (m Ω cm)